

## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings of claims in the application:

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1 1. (Original): A radially distributed serial control bus architecture, comprising:  
2 a controller;  
3 a plurality of connections, each connection having a first end and a second end,  
4 each of said first end of said each connection coupled to said controller; and  
5 a plurality of peripheral cards each peripheral card individually coupled to a  
6 second end of a respective dedicated one of said plurality of connections.

a 1 2. (Currently Amended): The architecture of claim 1 wherein each of said  
2 peripheral cards includes a transmit connection and a collision connection, and further,  
3 wherein each of said transmit and collision connections of each of said ~~for said each~~  
4 peripheral cards are connected to a separate second end of said respective dedicated one  
5 of said plurality of connections.

1 3. (Original): The architecture of claim 1 wherein each of said peripheral cards  
2 includes a transmit lead and a collision lead, and each of said transmit lead and said  
3 collision lead are separately coupled to said second end of said respective dedicated one  
4 of said plurality of connections.

1 4. (Original): The architecture of claim 1 further including a logic device  
2 provided between each of said peripheral cards and said controller.

1 5. (Original): The architecture of claim 4 wherein said logic device includes a  
2 field programmable gate array device.

1 6. (Original): The architecture of claim 4 wherein said logic device includes a  
2 plurality of drivers each dedicated to receive signals from a particular one of said plurality  
3 of peripheral cards, wherein said controller is configured to individually disable one or  
4 more of said plurality of drivers.

1 7. (Original): The architecture of claim 4 wherein said logic device includes:  
2 a control unit for generating a control signal;  
3 a plurality of OR gates each configured to perform an OR operation to said control  
4 signal and a signal received from a respective peripheral card; and  
5 an AND gate configured to perform an AND operation to outputs of said OR  
6 gates, and to provide an output AND signal to said controller.

1 8. (Original): The architecture of claim 1 wherein each of said plurality of  
2 connections is a hard wire connection.

1 9. (Original): The architecture of claim 1 wherein said controller is one of a MPC  
2 860 processor, a MPC 850 processor, and a MPC 8260 processor.

1 10. (Original): The architecture of claim 1 wherein said serial control bus is  
2 configured to operate at a frequency range between approximately 3 MHz and 6 MHz.

1 11. (Original): The architecture of claim 1 wherein each of said plurality of  
2 peripheral cards is separated from said system controller by a distance ranging from  
3 approximately one inch to seven feet.

1 12. (Original): The architecture of claim 1 wherein each of said plurality of  
2 peripheral cards are coupled to an optical data communications network, each configured  
3 to receive and transmit electrical and optical signals.

1 13. (Original): The architecture of claim 12 wherein said optical signals include  
2 one of OC-3, OC-12 and OC-48, and said electrical signals include one of STS-3, STS-12  
3 and STS-48.

1 14. (Original): The architecture of claim 1 wherein said serial control bus may be  
2 configured to support a bandwidth of approximately 6 Mbps.

1 15. (Original): The architecture of claim 1 wherein said serial control bus may be  
2 configured to support half duplex mode and full duplex mode communication.

1 16. (Original): A method of providing a radially distributed serial control bus  
2 architecture, comprising the steps of:  
3 connecting each of a first end of a plurality of connections to a controller; and  
4 individually connecting each of a plurality of peripheral cards to a second end of a  
5 respective dedicated one of said plurality of connections.

1 17. (Original): The method of claim 16 wherein said step of individually  
2 connecting includes the step of separately connecting a transmit connection and a  
3 collision connection of each of said peripheral cards to said second end of said respective  
4 dedicated one of said plurality of connections.

1 18. (Original): The method of claim 16 wherein said step of individually  
2 connecting includes the step of individually coupling a transmit lead and a collision lead  
3 of each of said peripheral cards to said second end of said respective dedicated one of  
4 said plurality of connections.

1 19. (Original): The method of claim 16 further including the step of providing a  
2 logic device between each of said peripheral cards and said controller.

1 20. (Original): The method of claim 16 wherein said logic device includes a field  
2 programmable gate array device.

1 21. (Original): The method of claim 16 wherein said step of providing said logic  
2 device includes the steps of:  
3 providing a plurality of drivers each dedicated to receive signals from a particular  
4 one of said plurality of peripheral cards; and

5 configuring said controller to individually disable one or more of said plurality of  
6 drivers.

1 22. (Original): The method of claim 21 wherein said step of providing said logic  
2 device includes the step of:  
3 generating a control signal;  
4 performing an OR operation to said control signal and a signal received from each  
5 peripheral card; and  
6 performing an AND operation to outputs of said OR operations and generating an  
7 output AND signal.

1 23. (Original): The method of claim 16 wherein each of said plurality of  
2 connections is a hard wire connection.

1 24. (Original): The method of claim 16 wherein said controller is one of a MPC  
2 860 processor, a MPC 850 processor, and a MPC 8260 processor.

1 25. (Original): The method of claim 16 wherein said serial control bus is  
2 configured to operate at a frequency range between approximately 3 MHz and 6 MHz.

1 26. (Original): The method of claim 16 wherein each of said plurality of  
2 connections is approximately one inch to seven feet in length.

1 27. (Original): The method of claim 16 further including the step of coupling each  
2 of said plurality of peripheral cards to an optical data communications network, and  
3 configuring said each peripheral card to receive and transmit electrical and optical  
4 signals.

1 28. (Original): The method of claim 27 wherein said optical signals include one of  
2 OC-3, OC-12 and OC-48; and said electrical signals include one of STS-3, STS-12 and  
3 STS-48.

1 29. (Original): The method of claim 16 wherein said serial control bus may be  
2 configured to support a bandwidth of approximately 6 Mbps.

1 30. (Original): The method of claim 16 wherein said serial control bus may be  
2 configured to support half duplex mode and full duplex mode communication.

1 31. (Currently Amended): A method of fault isolation in a serial control bus  
2 architecture, comprising the steps of:  
3 detecting a signal communication failure on a data control bus;  
4 performing a control bus integrity check responsive to the signal communication  
5 failure; and  
6 isolating the origin of said signal communication failure on said bus to a particular  
7 peripheral device.

1 32. (Original): The method of claim 31 wherein said communication failure  
2 includes a peripheral card lack of response to a system controller request or a background  
3 poll.

1 33. (Original): The method of claim 31 wherein said step of performing said bus  
2 integrity check includes the steps of:  
3 detecting a combined control bus signal; and  
4 determining whether a transmit signal from a peripheral device is continuously  
5 low.

1 34. (New): A radially distributed serial control bus to isolate data faults sent to  
2 a data bus, comprising:  
3 a plurality of peripheral cards to transmit data on the data bus; and  
4 a controller, coupled to the data bus and separately coupled to each of the plurality  
5 of peripheral cards, the controller performing an integrity check to isolate a  
6 fault to one of the plurality of peripheral cards.

1 35. (New): The control bus of claim 34, wherein the controller is configured to  
2 determine whether the fault occurred on one of the plurality of peripheral cards or on the  
3 controller.